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(54) **THIN FILM TRANSISTOR ARRAY PANEL AND ORGANIC LIGHT EMITTING DIODE DISPLAY INCLUDING THE SAME**

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(57) **ABSTRACT**

An exemplary embodiment of the present invention provides a thin film transistor array panel and an organic light emitting diode display including the same including a substrate, a semiconductor disposed on the substrate, a first gate insulation layer disposed on the semiconductor, and a first diffusion barrier layer disposed on the first gate insulation layer. A second diffusion barrier layer is disposed on a lateral surface of the first diffusion barrier layer. A first gate electrode is disposed on the first diffusion barrier layer. A source electrode and a drain electrode are connected to the semiconductor. The first diffusion barrier layer comprises a metal, and the second diffusion barrier layer comprises a metal oxide including the metal.

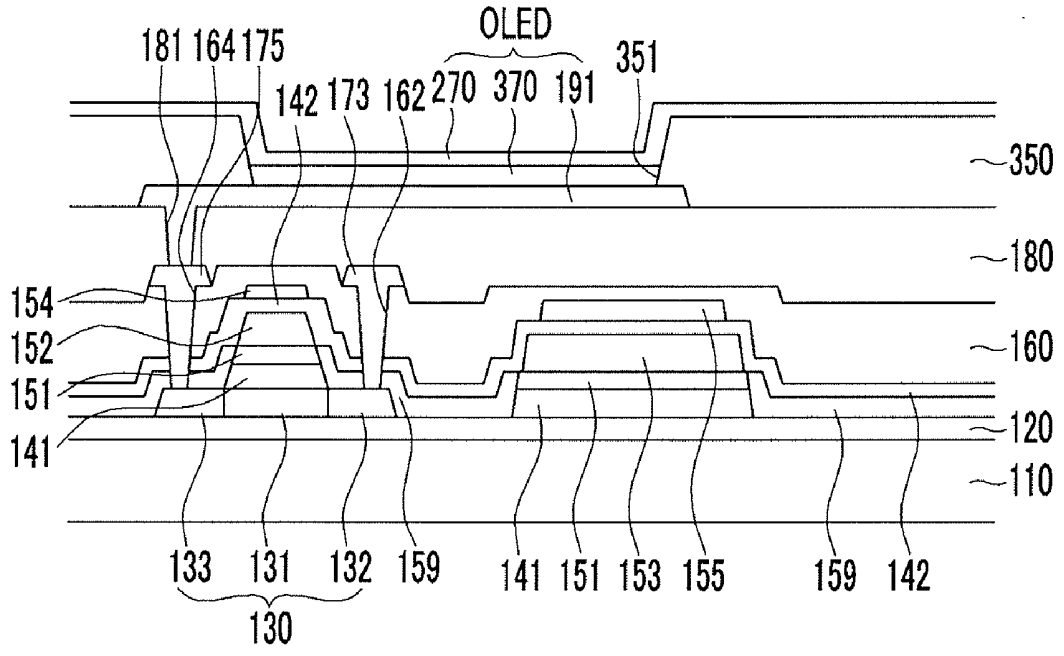

FIG. 1

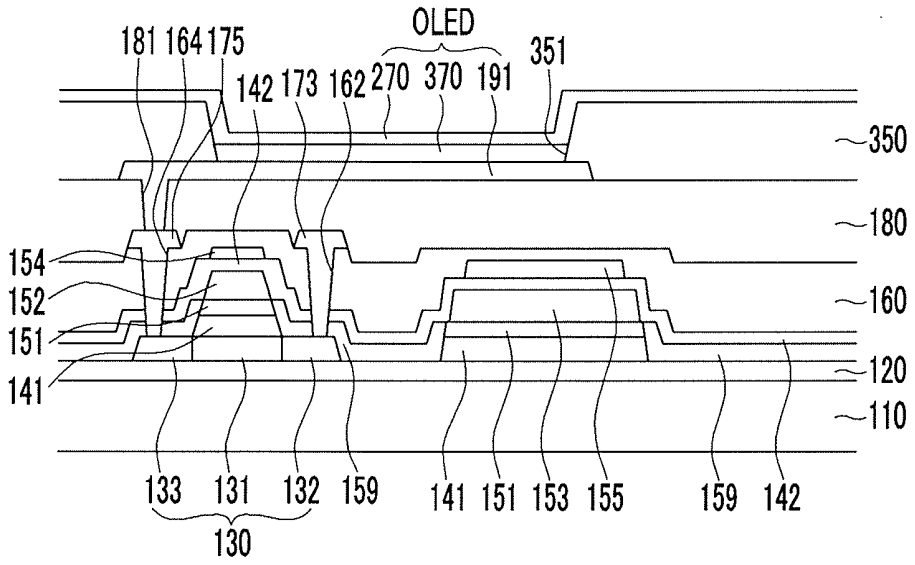
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FIG. 2

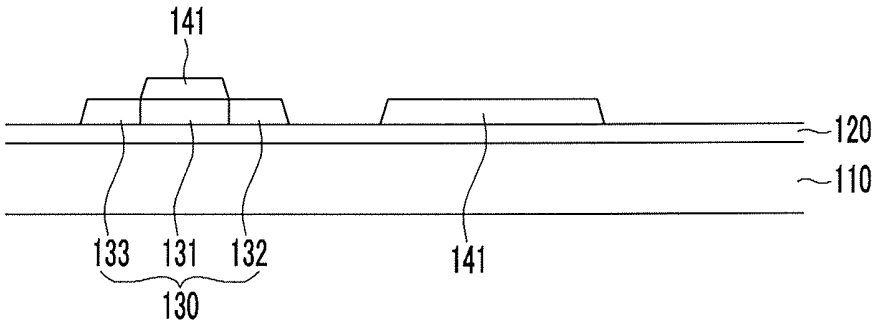

FIG. 3

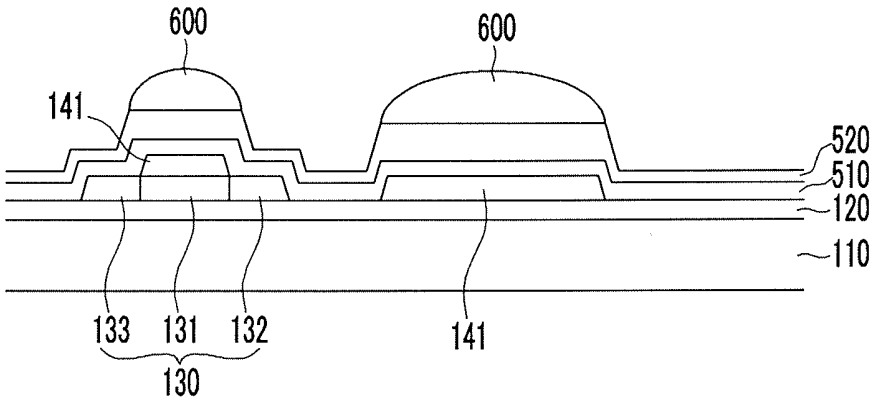

FIG. 4

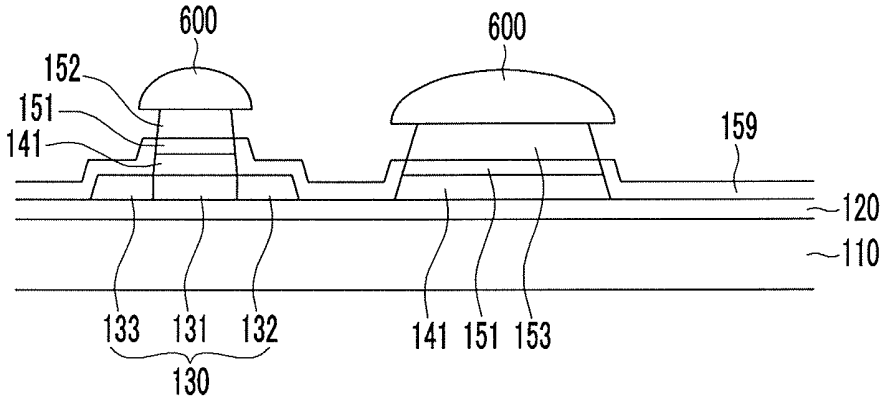

FIG. 5

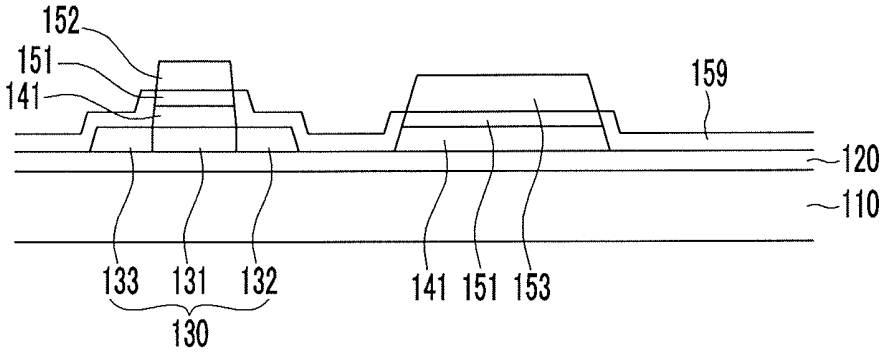

FIG. 6

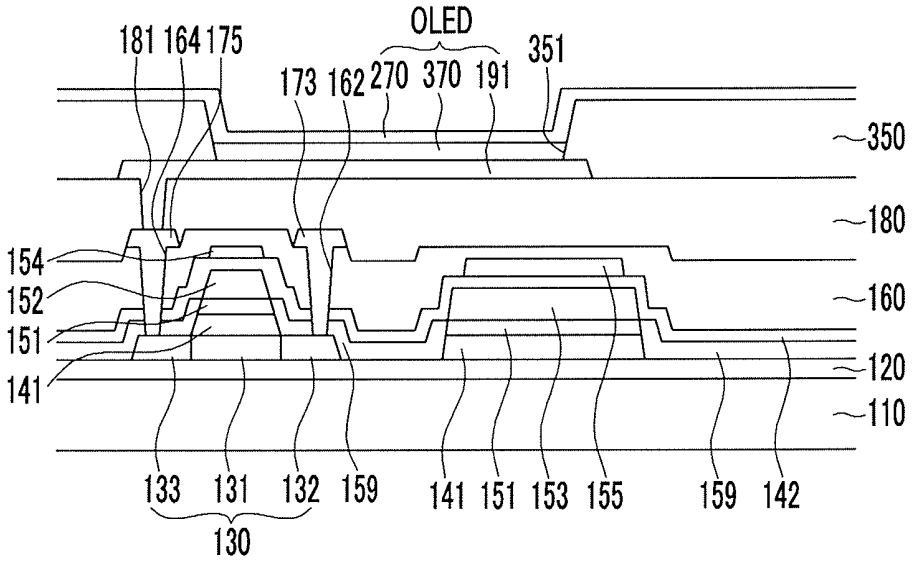
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FIG. 7

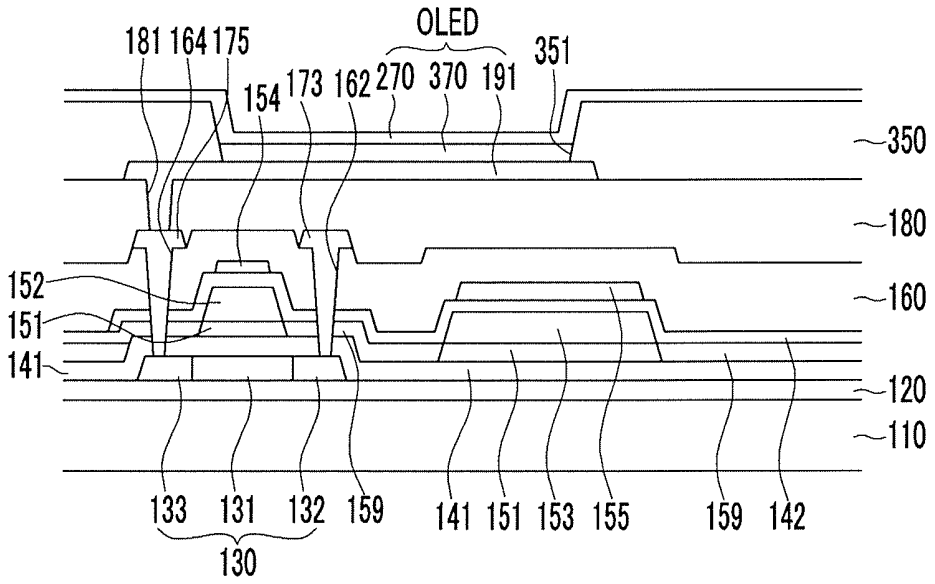
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FIG. 8

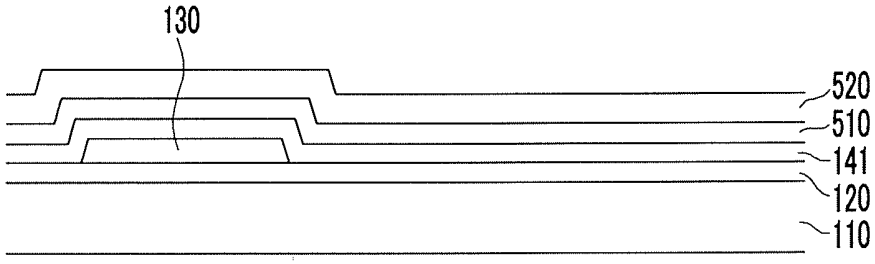

FIG. 9

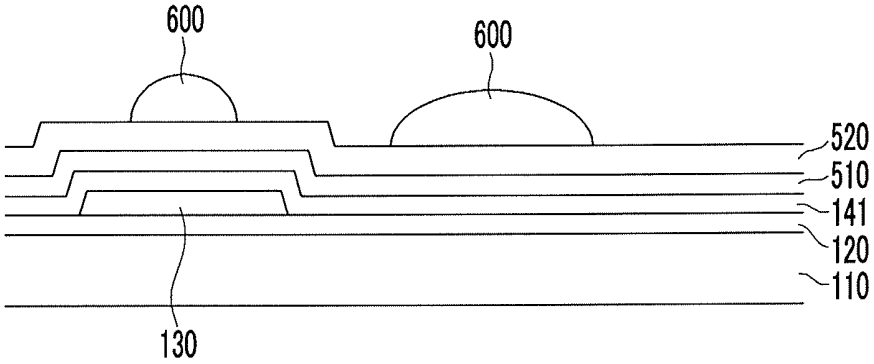

FIG. 10

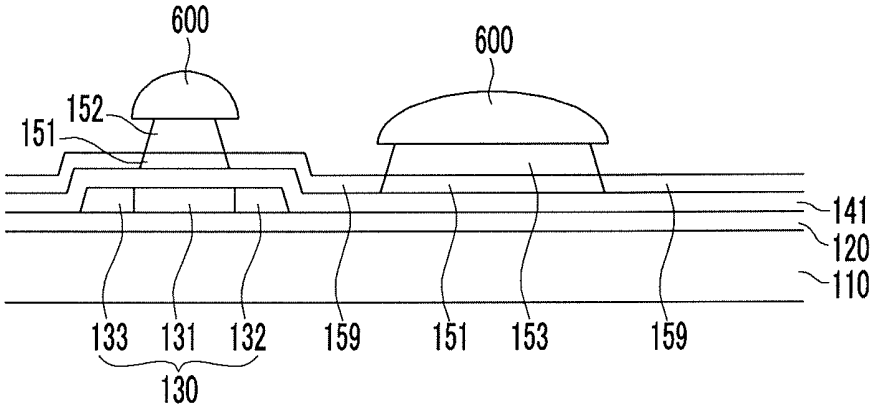

FIG. 11

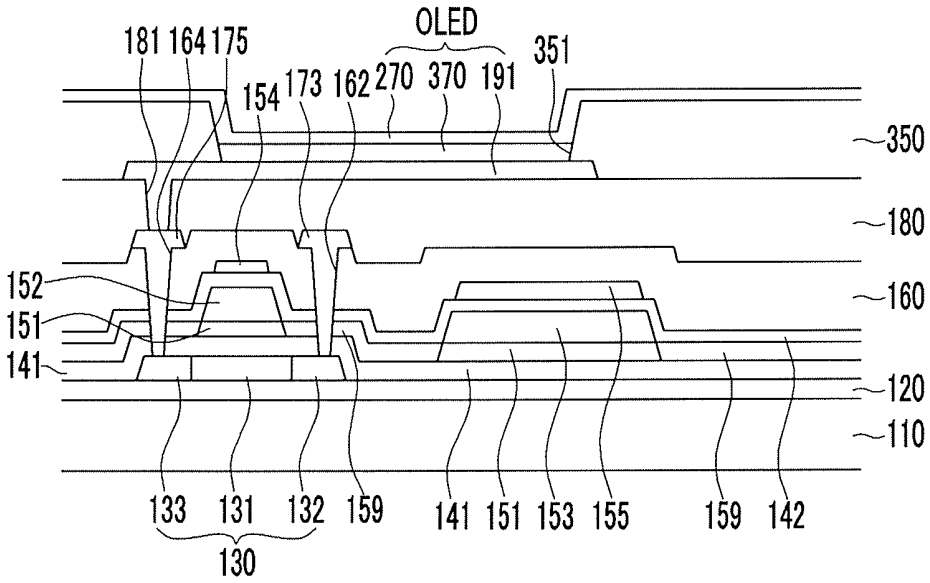
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FIG. 12

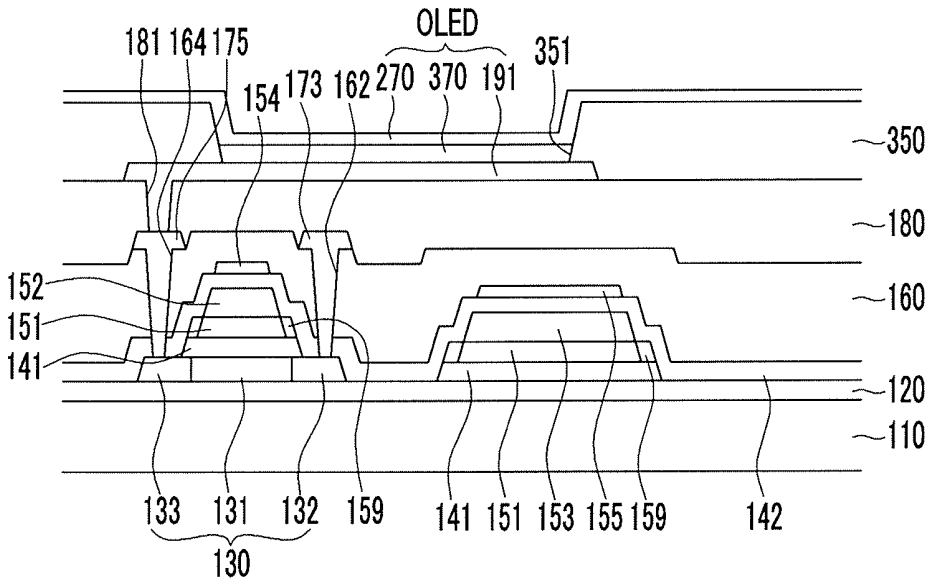
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FIG. 13

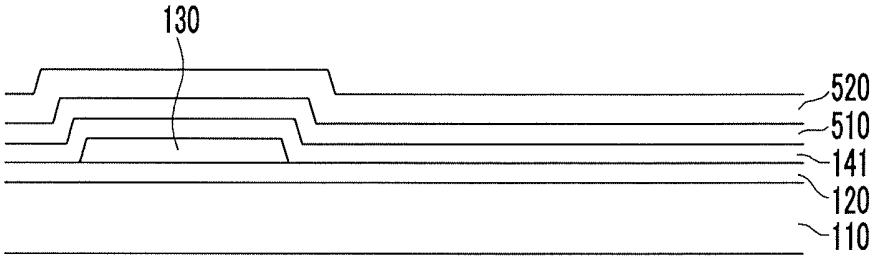


FIG. 14

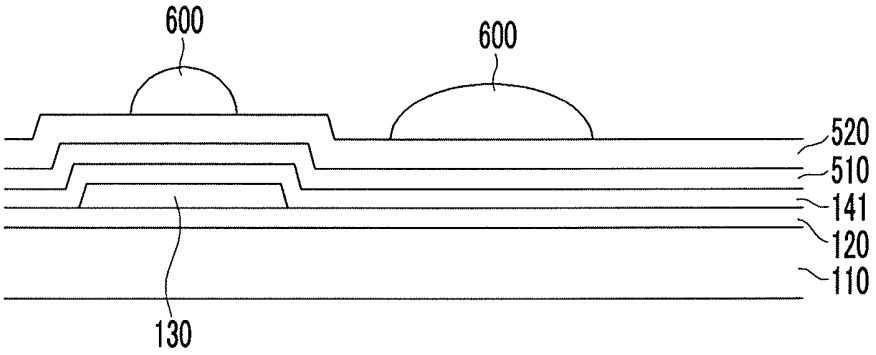


FIG. 15

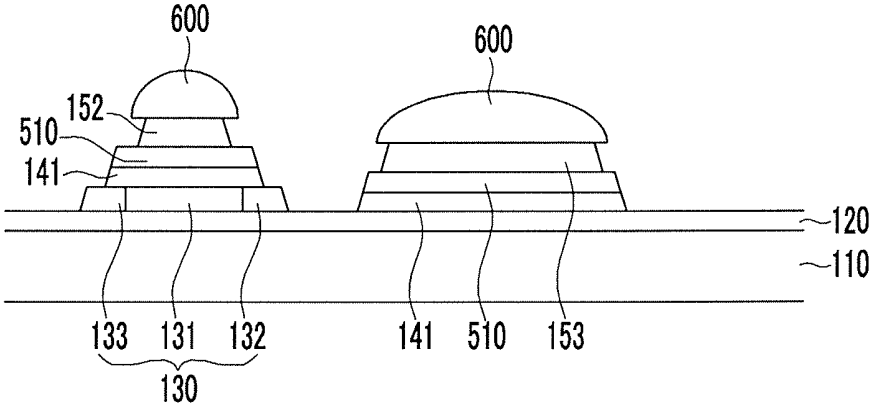


FIG. 16

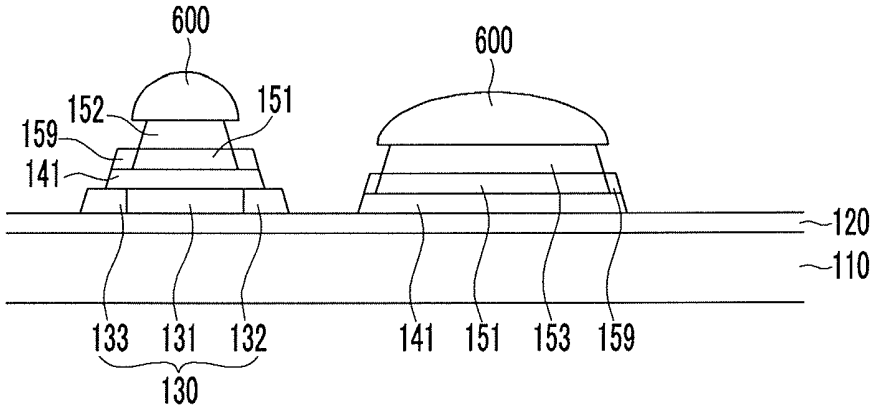
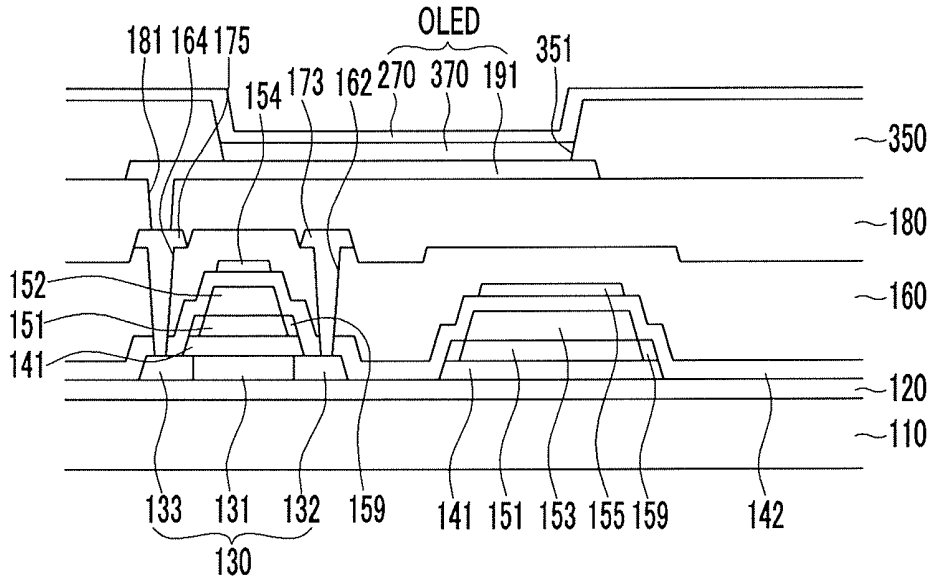


FIG. 17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THIN FILM TRANSISTOR ARRAY PANEL AND ORGANIC LIGHT EMITTING DIODE DISPLAY INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2015-0170781 filed in the Korean Intellectual Property Office on Dec. 2, 2015, the disclosure of which is incorporated by reference herein in its entirety.

[0002] 1. Technical Field

[0003] Exemplary embodiments of the present invention relate to a thin film transistor array panel, and more particularly to an organic light emitting diode display including the same.

[0004] 2. Discussion of Related Art

[0005] An organic light emitting diode display may include two electrodes and an organic emission layer disposed between the two electrodes. Electrons injected from one electrode and holes injected from the other electrode may combine to form excitons in the organic emission layer. When the excitons are changed from an excited state to a ground state, energy is released, thereby emitting light.

[0006] An organic light emitting diode display may include a plurality of pixels each of which may include an organic light emitting diode that is a self-emissive element. A plurality of transistors and at least one capacitor may be formed in each of the pixels to drive the organic light emitting diode. The transistors may include a switching transistor and a driving transistor.

[0007] The transistors may be top-gate type transistors in which a gate electrode is disposed on a semiconductor. The semiconductor may include an oxide semiconductor material, and the gate electrode may include a relatively low resistance metal such as copper.

SUMMARY

[0008] Exemplary embodiments of the present invention may provide a thin film transistor array panel and an organic light emitting diode display including the same.

[0009] An exemplary embodiment of the present invention provides a thin film transistor array panel including a substrate, a semiconductor disposed on the substrate, a first gate insulation layer disposed on the semiconductor, and a first diffusion barrier layer disposed on the first gate insulation layer. A second diffusion barrier layer is disposed on a lateral surface of the first diffusion barrier layer. A first gate electrode is disposed on the first diffusion barrier layer. A source electrode and a drain electrode are connected to the semiconductor. The first diffusion barrier layer includes a metal, and the second diffusion barrier layer includes a metal oxide including the metal.

[0010] Lateral edges of the first diffusion barrier layer and the first gate electrode may be substantially aligned with each other.

[0011] The semiconductor may include an oxide semiconductor material, and the first gate electrode may include copper.

[0012] The first diffusion barrier layer may include titanium, and the second diffusion barrier layer may include titanium oxide.

[0013] The semiconductor may include a channel region, and a source region and a drain region disposed on opposite sides of the channel region.

[0014] The first gate insulation layer, the first diffusion barrier layer, and the first gate electrode may overlap the channel region of the semiconductor. The second diffusion barrier layer may overlap the source region and the drain region of the semiconductor.

[0015] The second diffusion barrier layer may contact a lateral surface of the first gate insulation layer. The second diffusion barrier layer may be disposed directly on the source region and the drain region of the semiconductor.

[0016] The first gate insulation layer need not overlap the source region and the drain region of the semiconductor.

[0017] The second diffusion barrier layer may cover upper surfaces and lateral surfaces of the source region and the drain region of the semiconductor.

[0018] The second diffusion barrier layer may be substantially entirely overlapped with the source region and the drain region of the semiconductor.

[0019] The first gate insulation layer may be disposed directly on the channel region, the source region, and the drain region of the semiconductor. The second diffusion barrier layer may be disposed directly on the first gate insulation layer.

[0020] The second diffusion barrier layer may be substantially entirely overlapped with the source region and the drain region of the semiconductor.

[0021] A second gate insulation layer disposed on the first gate electrode, the second diffusion barrier layer, and the semiconductor may further be included. The second gate insulation layer may be disposed directly on the source region and the drain region of the semiconductor.

[0022] The second diffusion barrier layer may be partially overlapped with the source region and the drain region of the semiconductor.

[0023] An exemplary embodiment of the present invention may provide a thin film transistor array panel that may include a second gate insulation layer disposed on the first gate electrode and the second diffusion barrier layer, a second gate electrode disposed on the second gate insulation layer, and an interlayer insulation layer disposed on the second gate electrode and the second gate insulation layer. The source electrode and the drain electrode may be disposed on the interlayer insulation layer.

[0024] The second gate insulation layer may include silicon nitride.

[0025] An exemplary embodiment of the present invention provides an organic light emitting diode display including a substrate, a semiconductor disposed on the substrate, a first gate insulation layer disposed on the semiconductor, and a first diffusion barrier layer disposed on the first gate insulation layer. A second diffusion barrier layer is disposed on a lateral surface of the first diffusion barrier layer. A first gate electrode is disposed on the first diffusion barrier layer. A source electrode and a drain electrode are connected to the semiconductor. A first electrode is connected to the drain electrode. An organic emission layer is disposed on the first electrode, and a second electrode is disposed on the organic emission layer. The first diffusion barrier layer includes a metal, and the second diffusion barrier layer includes a metal oxide including the metal.

[0026] Lateral edges of the first diffusion barrier layer and the first gate electrode may be substantially aligned with each other.

[0027] The semiconductor may include an oxide semiconductor material. The first gate electrode may include copper. The first diffusion barrier layer may include titanium. The second diffusion barrier layer may include titanium oxide.

[0028] The semiconductor may include a channel region and a source region and a drain region disposed on opposite sides of the channel region. The first gate insulation layer, the first diffusion barrier layer, and the first gate electrode may overlap the channel region of the semiconductor. The second diffusion barrier layer may overlap the source region and the drain region of the semiconductor.

[0029] In the thin film transistor array panel and the organic light emitting diode display including the same according to some exemplary embodiments of the present invention, the edges of the first diffusion barrier layer and the first gate electrode may be substantially aligned with each other by forming the second diffusion barrier layer which contacts the lateral surface of the first diffusion barrier layer. Thus, performance of the thin film transistor may be prevented from deteriorating. The first diffusion barrier layer might not be protruded more than the first gate electrode, and thus a reduction in performance of the thin film transistor according to an exemplary embodiment of the present invention may be reduced or prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The above and other features of the inventive concept will become more apparent by describing in detail exemplary embodiments thereof, with reference to the accompanying, in which:

[0031] FIG. **1** is a cross-sectional view illustrating an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0032] FIG. **2** to FIG. **6** are process cross-sectional views illustrating a manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0033] FIG. **7** is a cross-sectional view illustrating an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0034] FIG. **8** to FIG. **11** are process cross-sectional views illustrating a manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0035] FIG. **12** is a cross-sectional view illustrating an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0036] FIG. **13** to FIG. **17** are process cross-sectional views illustrating a manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0037] Exemplary embodiments of the present invention will be described in more detail below with reference to the accompanying drawings, in which exemplary embodiments of the present invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

[0038] In the drawings, the thicknesses of layers, films, panels, or regions may be exaggerated for clarity. Like reference numerals may refer to like elements throughout the specification and drawings. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it may be directly on the other element or intervening elements may be present.

[0039] An organic light emitting diode display according to an exemplary embodiment of the present invention will be described in more detail below with reference to FIG. **1**.

[0040] FIG. **1** is a cross-sectional view illustrating an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0041] Referring to FIG. **1**, the organic light emitting diode display according to an exemplary embodiment of the present invention may include a substrate **110**, a semiconductor **130** disposed on the substrate **110**, a first gate insulation layer **141** disposed on the semiconductor **130**, a first diffusion barrier layer **151** disposed on the first gate insulation layer **141**, a second diffusion barrier layer **159** in contact with a lateral surface of the first diffusion barrier layer **151**, and a first gate electrode **152** disposed on the first diffusion barrier layer **151**.

[0042] The substrate **110** may include an insulating substrate. The insulating substrate may include glass, quartz, ceramic, or plastic. However, exemplary embodiments of the present invention are not limited thereto, and the substrate **110** may include a metal substrate. The metal substrate may include stainless steel.

[0043] A buffer layer **120** may be disposed on the substrate **110**. The buffer layer **120** may include a silicon nitride (SiN_x) or a silicon oxide (SiO_x). The buffer layer **120** may reduce or prevent impurities or moisture from infiltrating the substrate **110** (e.g., while planarizing a surface of the substrate **110**). According to an exemplary embodiment of the present invention, the buffer layer **120** may be omitted.

[0044] The semiconductor **130** may be disposed on the buffer layer **120**. The semiconductor **130** may include an oxide semiconductor material. The semiconductor **130** may include a channel region **131** to which an impurity is not doped, and contact doping regions **132** and **133** disposed on opposite sides of the channel region **131** and to which an impurity is doped. The contact doping regions **132** and **133** may include a source region **132** and a drain region **133**. The impurity may be selected depending on a type of a thin film transistor.

[0045] The first gate insulation layer **141** may include silicon nitride (SiN_x) or silicon oxide (SiO_x). The first gate insulation layer **141** may overlap the channel region **131** of the semiconductor **130**. The first gate insulation layer **141** need not overlap the source region **132** and the drain region **133** of the semiconductor **130**.

[0046] The first diffusion barrier layer **151** may include a metal. For example, the first diffusion barrier layer **151** may include titanium (Ti). The first diffusion barrier layer **151** may overlap the channel region **131** of the semiconductor **130**. The first diffusion barrier layer **151** need not overlap the source region **132** and the drain region **133** of the semiconductor **130**.

[0047] The second diffusion barrier layer **159** may include a metal oxide including the same metal as the first diffusion barrier layer **151**. For example, the second diffusion barrier

layer **159** may include titanium oxide (TiO_x). The second diffusion barrier layer **159** may overlap the source region **132** and the drain region **133** of the semiconductor **130**. The second diffusion barrier layer **159** may be disposed directly on the source region **132** and the drain region **133** of the semiconductor **130**. The second diffusion barrier layer **159** may cover upper surfaces and lateral surfaces of the source region **132** and the drain region **133** of the semiconductor **130**. The second diffusion barrier layer **159** may be substantially entirely overlapped with the source region **132** and the drain region **133** of the semiconductor **130**. The second diffusion barrier layer **159** may contact a lateral surface of the first gate insulation layer **141** and may be disposed on the buffer layer **120**.

[0048] The first gate electrode **152** may include copper (Cu). The first gate electrode **152** may overlap the channel region **131** of the semiconductor **130**. Planar shapes of the first gate electrode **152** and the first diffusion barrier layer **151** may be substantially identical to each other. The first gate electrode **152** and the first diffusion barrier layer **151** may have a substantially identical planar shape at a contacting surface between the first gate electrode **152** and the first diffusion barrier layer **151**. Lateral surfaces of the first gate electrode **152** and the first diffusion barrier layer **151** may have a tapered shape, and thus, planar shapes of the first gate electrode **152** and the first diffusion barrier layer **151** may be substantially identical to each other. However, according to an exemplary embodiment of the present invention planar sizes of the first gate electrode **152** and the first diffusion barrier layer **151** may be slightly different from each other. Thus, lateral edges of the first gate electrode **152** and the first diffusion barrier layer **151** may be substantially aligned with each other.

[0049] A second gate insulation layer **142** may be disposed on the first gate electrode **152** and the second diffusion barrier layer **159**. The second gate insulation layer **142** may include silicon nitride (SiN_x).

[0050] In an exemplary embodiment of the present invention, the first gate electrode **152** may include copper (Cu). The second gate insulation layer **142** may be formed after the first gate electrode **152** is formed. Since the second gate insulation layer **142** may include silicon nitride (SiN_x), oxidation of copper may be reduced or prevented during a process of forming the second gate insulation layer **142**. Since the first diffusion barrier layer **151** may be disposed under the first gate electrode **152**, a diffusion of hydrogen into the semiconductor **130** during the process of forming the second gate insulation layer **142** may be reduced or prevented. The semiconductor **130** may be an oxide semiconductor. The second diffusion barrier layer **159** contacting the first diffusion barrier layer **151** may include a metal oxide instead of a metallic material, and edges of the first diffusion barrier layer **151** and the first gate electrode **152** may substantially coincide with each other. Thus, a relatively high current may be prevented from flowing at an edge of the first diffusion barrier layer **151**. Thus, performance of the thin film transistor may be prevented from deteriorating.

[0051] A second gate electrode **154** may be disposed on the second gate insulation layer **142**. The second gate electrode **154** may overlap the first gate electrode **152**.

[0052] An interlayer insulation layer **160** may be disposed on the second gate electrode **154** and the second gate insulation layer **142**.

[0053] Contact holes **162** and **164** exposing at least a part of the semiconductor **130** may be formed in the second diffusion barrier layer **159**, the second gate insulation layer **142**, and the interlayer insulation layer **160**. The contact holes **162** and **164** may expose the contact doping regions **132** and **133** of the semiconductor **130**.

[0054] A source electrode **173** and a drain electrode **175** may be disposed on the interlayer insulation layer **160**. The source electrode **173** may be connected to the source region **132** of the semiconductor **130** through the contact hole **162**, and the drain electrode **175** may be connected to the drain region **133** of the semiconductor **130** through the contact hole **164**.

[0055] Thus, the semiconductor **130**, the first gate electrode **152**, the source electrode **173**, and the drain electrode **175** may be included in one thin film transistor. The thin film transistor may be a switching transistor or a driving transistor. The substrate **110** in which the thin film transistor is formed may be referred to as a thin film transistor array panel.

[0056] A passivation layer **180** may be disposed on the interlayer insulation layer **160**, the source electrode **173**, and the drain electrode **175**. A contact hole **181** may be formed in the passivation layer **180** to expose at least a part of the drain electrode.

[0057] A pixel electrode **191** may be disposed on the passivation layer **180**. The pixel electrode **191** may include a transparent conductive material such as indium-tin oxide (ITO), indium-zinc oxide (IZO), zinc oxide (ZnO), or indium oxide (In_2O_3), or a reflective metal such as lithium (Li), calcium (Ca), lithium fluoride/calcium (LiF/Ca), lithium fluoride/aluminum (LiF/Al), aluminum (Al), silver (Ag), magnesium (Mg), or gold (Au). The pixel electrode **191** may be electrically connected to the drain electrode **175** through the contact hole **181** to serve as an anode of an organic light emitting diode (OLED).

[0058] A pixel definition layer **350** may be disposed on the passivation layer **180** and an edge portion of the pixel electrode **191**. The pixel definition layer **350** may include a pixel opening **351** exposing the pixel electrode **191**. The pixel definition layer **350** may include a resin such as a polyacrylate, or a polyimide, or a silica-based inorganic material.

[0059] An organic emission layer **370** may be formed in the pixel opening **351** of the pixel definition layer **350**. The organic emission layer **370** may include at least one of an emission layer, a hole-injection layer (HIL), a hole-transport layer (HTL), an electron-transport layer (ETL), and an electron-injection layer (EIL).

[0060] The organic emission layer **370** may include a red organic emission layer emitting red light, a green organic emission layer emitting green light, and a blue organic emission layer emitting blue light. According to an exemplary embodiment of the present invention, the red organic emission layer, the green organic emission layer, and the blue organic emission layer may be respectively formed in a red pixel, a green pixel, and a blue pixel to display a color image.

[0061] According to an exemplary embodiment of the present invention, the organic emission layer **370** may display a color image by stacking a red organic emission layer, a green organic emission layer, and a blue organic emission layer in each of a red pixel, a green pixel, and a blue pixel to form a red filter, a green filter, and a blue filter

for each pixel. According to an exemplary embodiment of the present invention, a color image may be displayed by forming a white organic emission layer emitting white light in each of the red pixel, the green pixel, and the blue pixel to form a red filter, a green filter, and a blue filter for each pixel. When a color image is displayed by using the white organic emission layer and the color filters, a deposition mask for depositing a red organic emission layer, a green organic emission layer, and a blue organic emission layer on each of the pixels (e.g., the red pixel, the green pixel, and the blue pixel) may be omitted.

[0062] The white organic emission layer may include one organic emission layer, or may include a plurality of organic emission layers to emit white light. Alternatively, the white organic emission layer may include at least one yellow organic emission layer and at least one blue organic emission layer to emit white light, by combining at least one cyan organic emission layer and at least one red organic emission layer to emit white light, by combining at least one magenta organic emission layer and at least one green organic emission layer to emit white light, and the like.

[0063] A common electrode **270** may be disposed on the pixel definition layer **350** and the organic emission layer **370**. The common electrode **270** may include a transparent conductive material such as indium-tin oxide (ITO), indium-zinc oxide (IZO), zinc oxide (ZnO), indium oxide (In_2O_3), or the like, or a reflective metal such as lithium (Li), calcium (Ca), lithium fluoride/calcium (LiF/Ca), lithium fluoride/aluminum (LiF/Al), aluminum (Al), silver (Ag), magnesium (Mg), or gold (Au). The common electrode **270** may serve as a cathode of an organic light emitting diode (OLED). The pixel electrode **191**, the organic emission layer **370**, and the common electrode **270** may be included in the organic light emitting diode (OLED).

[0064] An organic light emitting diode display according to an exemplary embodiment of the present invention may include a first storage electrode **153** disposed on the substrate **110** and a second storage electrode **155** overlapping the first storage electrode **153**.

[0065] The first diffusion barrier layer **151**, the first gate insulation layer **141**, and the buffer layer **120** may be disposed under the first storage electrode **153**. The second gate insulation layer **142** may be disposed between the first storage electrode **153** and the second storage electrode **155**. The first storage electrode **153** and the second storage electrode **155** may be included in a storage capacitor together with the second gate insulation layer **142** as a dielectric material.

[0066] A manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention will be described in more detail below with reference to FIG. **2** to FIG. **6**.

[0067] FIG. **2** to FIG. **6** are process cross-sectional views illustrating a manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0068] Referring to FIG. **2**, the buffer layer **120** may be formed by depositing silicon nitride (SiN_x) or silicon oxide (SiO_x) on the substrate **110**.

[0069] The semiconductor **130** may be formed by depositing an oxide semiconductor material on the buffer layer **120** and then patterning it.

[0070] The first gate insulation layer **141** may be formed by depositing silicon nitride (SiN_x) or silicon oxide (SiO_x) on the semiconductor **130** and the buffer layer **120** and then patterning it.

[0071] The semiconductor **130** may include the channel region **131**, and the source region **132** and the drain region **133** disposed on opposite sides of the channel region **131**. The first gate insulation layer **141** may overlap the channel region **131** of the semiconductor **130**.

[0072] Referring to FIG. **3**, a first metallic material layer **510** and a second metallic material layer **520** may be sequentially deposited on the first gate insulation layer **141**, the semiconductor **130**, and the buffer layer **120**. The first metallic material layer **510** may include titanium (Ti), and the second metallic material layer **520** may include copper (Cu).

[0073] A photoresist pattern **600** may be formed by coating a photosensitive material on the second metallic material layer **520** and then patterning it.

[0074] Referring to FIG. **4**, the first gate electrode **152** and the first storage electrode **153** may be formed by etching the second metallic material layer **520** using the photoresist pattern **600** as a mask.

[0075] The second diffusion barrier layer **159** may be formed by oxidizing the first metallic material layer **510** using the photoresist pattern **600** as a mask. A part of the first metallic material layer **510**, which is disposed under the photoresist pattern **600**, and thus might not be oxidized, may serve as the first diffusion barrier layer **151**.

[0076] Thus, the first diffusion barrier layer **151** may include titanium (Ti), and the second diffusion barrier layer **159** may include titanium oxide (TiO_x).

[0077] In an exemplary embodiment of the present invention, the photoresist pattern **600** may be employed as a mask to etch the second metallic material layer **520** and to oxidize the first metallic material layer **510**. Thus, planar shapes of the first gate electrode **152** and the first diffusion barrier layer **151** may be substantially identical to each other. Edges of the first gate electrode **152** and the first diffusion barrier layer **151** may substantially coincide with each other, and the first diffusion barrier layer **151** need not protrude more than the first gate electrode **152**. Thus, a relatively high current may be reduced or prevented from being generated at an edge of the first diffusion barrier layer **151**, and performance of the thin film transistor may be prevented from deteriorating.

[0078] Referring to FIG. **5**, the photoresist pattern **600** may be removed.

[0079] Referring to FIG. **6**, the second gate insulation layer **142** may be formed by depositing silicon nitride (SiN_x) on the first gate electrode **152** and the second diffusion barrier layer **159**.

[0080] The second gate electrode **154** overlapping the first gate electrode **152** and the second storage electrode **155** formed overlapping the first storage electrode **153** may be formed by depositing a metal material on the second gate insulation layer **142** and then patterning it.

[0081] The interlayer insulation layer **160** may be disposed on the second storage electrode **155** and the second gate insulation layer **142**. The contact holes **162** and **164** exposing the source region **132** and the drain region **133** of the semiconductor **130** may be formed by patterning the interlayer insulation layer **160**.

[0082] The source electrode **173** and the drain electrode **175** may be formed by depositing a metal material on the interlayer insulation layer **160** and then patterning it. The source electrode **173** and the drain electrode **175** may be respectively connected to the source region **132** and the drain region **133** of the semiconductor **130** through the contact holes **162** and **164**.

[0083] The passivation layer **180** may be disposed on the source electrode **173**, the drain electrode **175**, and the interlayer insulation layer **160**. The contact hole **181** exposing the drain electrode **175** may be formed by patterning the passivation layer **180**.

[0084] The pixel electrode **191** may be formed by depositing a metal material on the passivation layer **180** and then patterning it. The pixel electrode **191** may be connected to the drain electrode **175** through the contact hole **181**.

[0085] The pixel definition layer **350** may be formed by depositing an insulating material on the pixel electrode **191** and the passivation layer **180** and then patterning it. The pixel definition layer **350** may include the pixel opening **351** formed to expose the pixel electrode **191**.

[0086] The organic emission layer **370** may be formed in the pixel opening **351**. The common electrode **270** may be formed by depositing a metal material on the organic emission layer **370** and the pixel definition layer **350** and then patterning it.

[0087] An organic light emitting diode display according to an exemplary embodiment of the present invention will be described in more detail below with reference to FIG. **7**.

[0088] Since the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **7** may include substantially identical elements to those of the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **1**, duplicative descriptions may be omitted. Referring to FIG. **7**, a first gate insulation layer may cover a source region and a drain region as well as a channel region of a semiconductor. The semiconductor will be described in more detail below with reference to FIG. **7**.

[0089] FIG. **7** is a cross-sectional view illustrating the organic light emitting diode display according to an exemplary embodiment of the present invention.

[0090] Referring to FIG. **7**, the organic light emitting diode display according to an exemplary embodiment of the present invention may include the substrate **110**, the semiconductor **130** disposed on the substrate **110**, the first gate insulation layer **141** disposed on the semiconductor **130**, the first diffusion barrier layer **151** disposed on the first gate insulation layer **141**, the second diffusion barrier layer **159** in contact with a lateral surface of the first diffusion barrier layer **151**, and the first gate electrode **152** disposed on the first diffusion barrier layer **151**.

[0091] According to an exemplary embodiment of the present invention, the first gate insulation layer **141** may overlap the channel region **131** of the semiconductor **130**, and might not overlap the source region **132** and the drain region **133**. However, according to another exemplary embodiment of the present invention, the first gate insulation layer **141** may overlap the channel region **131**, the source region **132**, and the drain region **133** of the semiconductor **130**. The first gate insulation layer **141** may be disposed directly on the channel region **131**, the source region **132**, and the drain region **133** of the semiconductor **130**. The first gate insulation layer **141** may cover both of an upper surface and a lateral surface of the semiconductor **130**.

[0092] According to an exemplary embodiment of the present invention, the second diffusion barrier layer **159** may be disposed directly on the source region **132** and the drain region **133** of the semiconductor **130**. However, according to another exemplary embodiment of the present invention, the first gate insulation layer **141** may be disposed between the second diffusion barrier layer **159** and the source region **132** of the semiconductor **130** and between the second diffusion barrier layer **159** and the drain region **133** of the semiconductor **130**. Thus, the second diffusion barrier layer **159** may be disposed directly on the first gate insulation layer **141**.

[0093] A manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention will be described in more detail below with reference to FIG. **8** to FIG. **11**.

[0094] Since the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **8** to FIG. **11** may include substantially identical elements to those of the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **2** to FIG. **6**, duplicative descriptions may be omitted.

[0095] FIG. **8** to FIG. **11** are process cross-sectional views illustrating a manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0096] Referring to FIG. **8**, the buffer layer **120** may be disposed on the substrate **110**, and the semiconductor **130** may be disposed on the buffer layer **120**.

[0097] The first gate insulation layer **141**, the first metallic material layer **510**, and the second metallic material layer **520** may be sequentially deposited on the semiconductor **130** and the buffer layer **120**.

[0098] Referring to FIG. **9**, the photoresist pattern **600** may be formed by coating a photosensitive material on the second metallic material layer **520** and then patterning it.

[0099] Referring to FIG. **10**, the first gate electrode **152** and the first storage electrode **153** may be formed by etching the second metallic material layer **520** using the photoresist pattern **600** as a mask.

[0100] The second diffusion barrier layer **159** may be formed by oxidizing the first metallic material layer **510** using the photoresist pattern **600** as a mask. A part of the first metallic material layer **510**, which is disposed under the first gate electrode **152** and the first storage electrode **153** and thus might not be oxidized, may serve as the first diffusion barrier layer **151**.

[0101] The first diffusion barrier layer **151** may include titanium (Ti), and the second diffusion barrier layer **159** may include titanium oxide (TiO_x).

[0102] The photoresist pattern **600** may then be removed, and the second gate insulation layer **142**, the second gate electrode **154**, the interlayer insulation layer **160**, the source electrode **173**, the drain electrode **175**, the passivation layer **180**, the pixel electrode **191**, the pixel definition layer **350**, the organic emission layer **370**, and the common electrode **270** may be sequentially formed (see, e.g., FIG. **11**).

[0103] An organic light emitting diode display according to an exemplary embodiment of the present invention will be described in more detail below with reference to FIG. **12**.

[0104] Since the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **12** may include substantially identical elements to those of the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **1**, duplicative descriptions may be omitted. A source region and a drain region of a semiconductor may be partially rather than entirely overlapped with a second diffusion barrier layer. The semiconductor will be described below in more detail.

[0105] FIG. **12** is a cross-sectional view illustrating an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0106] Referring to FIG. **12**, the organic light emitting diode display according to an exemplary embodiment of the present invention may include the substrate **110**, the semiconductor **130** disposed on the substrate **110**, the first gate insulation layer **141** disposed on the semiconductor **130**, the first diffusion barrier layer **151** disposed on the first gate insulation layer **141**, the second diffusion barrier layer **159** contacting a lateral surface of the first diffusion barrier layer **151**, and the first gate electrode **152** disposed on the first diffusion barrier layer **151**.

[0107] According to an exemplary embodiment of the present invention, the second diffusion barrier layer **159** may cover upper surfaces and lateral surfaces of the source region **132** and the drain region **133** of the semiconductor **130**, and may be substantially entirely overlapped with the source region **132** and the drain region **133** of the semiconductor **130**. According to another exemplary embodiment of the present invention, the second diffusion barrier layer **159** may be partially overlapped with the source region **132** and the drain region **133** of the semiconductor **130**. Most of the source region **132** and the drain region **133** of the semiconductor **130** might not be covered with the second diffusion barrier layer **159**.

[0108] The second gate insulation layer **142** may be disposed on the first gate electrode **152**, the second diffusion barrier layer **159**, and the semiconductor **130**. The second gate insulation layer **142** may be disposed directly on the source region **132** and the drain region **133** of the semiconductor **130**.

[0109] A manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention will be described in more detail below with reference to FIG. **13** to FIG. **17**.

[0110] Since the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **13** to FIG. **17** may include substantially identical elements to those of the organic light emitting diode display according to an exemplary embodiment of the present invention described with reference to FIG. **2** to FIG. **6**, duplicative descriptions may be omitted.

[0111] FIG. **13** to FIG. **17** are process cross-sectional views illustrating a manufacturing method of an organic light emitting diode display according to an exemplary embodiment of the present invention.

[0112] Referring to FIG. **13**, the buffer layer **120** may be disposed on the substrate **110**, and the semiconductor **130** may be disposed on the buffer layer **120**.

[0113] The first gate insulation layer **141**, the first metallic material layer **510**, and the second metallic material layer **520** may be sequentially deposited on the semiconductor **130** and the buffer layer **120**.

[0114] Referring to FIG. **14**, the photoresist pattern **600** may be formed by coating a photosensitive material on the second metallic material layer **520** and then patterning it.

[0115] Referring to FIG. **15**, the first gate electrode **152** and the first storage electrode **153** may be formed by jointly etching the second metallic material layer **520** and the first metallic material layer **510** using the photoresist pattern **600** as a mask. The second metallic material layer **520** and the first metallic material layer **510** may be jointly etched by a wet etching method. A part of the first metallic material layer **510** may be protruded more than the first gate electrode **152** because of a difference between an etching rate of the first metallic material layer **510** and an etching rate of the second metallic material layer **520**.

[0116] The first gate insulation layer **141** is etched by using the photoresist pattern **600** as a mask. The first gate insulation layer **141** may be etched by a dry etching method.

[0117] Referring to FIG. **16**, the second diffusion barrier layer **159** may be formed by oxidizing the first metallic material layer **510** using the photoresist pattern **600** as a mask. A part of the first metallic material layer **510** which is disposed under the first gate electrode **152** and the first storage electrode **153** and thus might not be oxidized may serve as the first diffusion barrier layer **151**.

[0118] The first diffusion barrier layer **151** may include titanium (Ti), and the second diffusion barrier layer **159** may include titanium oxide (TiO_x).

[0119] The photoresist pattern **600** may be removed, and the second gate insulation layer **142**, the second gate electrode **154**, the interlayer insulation layer **160**, the source electrode **173**, the drain electrode **175**, the passivation layer **180**, the pixel electrode **191**, the pixel definition layer **350**, the organic emission layer **370**, and the common electrode **270** may be sequentially formed (see, e.g., FIG. **17**).

[0120] While the present invention has been shown and described with reference to the exemplary embodiments thereof, it will be apparent to those of ordinary skill in the art that various changes in form and detail may be made thereto without departing from the spirit and scope of the present invention.

What is claimed is:

1. A thin film transistor array panel comprising:

a substrate;

a semiconductor disposed on the substrate;

a first gate insulation layer disposed on the semiconductor;

a first diffusion barrier layer disposed on the first gate insulation layer;

a second diffusion barrier layer disposed on a lateral surface of the first diffusion barrier layer;

a first gate electrode disposed on the first diffusion barrier layer; and

a source electrode and a drain electrode connected to the semiconductor,

wherein the first diffusion barrier layer comprises a metal, and the second diffusion barrier layer comprises a metal oxide including the metal.

2. The thin film transistor array panel of claim **1**, wherein lateral edges of the first diffusion barrier layer and the first gate electrode are substantially aligned with each other.

3. The thin film transistor array panel of claim 2, wherein the semiconductor includes an oxide semiconductor material, and the first gate electrode includes copper.

4. The thin film transistor array panel of claim 3, wherein the first diffusion barrier layer includes titanium, and the second diffusion barrier layer includes titanium oxide.

5. The thin film transistor array panel of claim 1, wherein the semiconductor includes a channel region, and a source region and a drain region disposed on opposite sides of the channel region.

6. The thin film transistor array panel of claim 5, wherein the first gate insulation layer, the first diffusion barrier layer, and the first gate electrode overlap the channel region of the semiconductor, and

wherein the second diffusion barrier layer overlaps the source region and the drain region of the semiconductor.

7. The thin film transistor array panel of claim 6, wherein the second diffusion barrier layer contacts a lateral surface of the first gate insulation layer, and wherein the second diffusion barrier layer is disposed directly on the source region and the drain region of the semiconductor.

8. The thin film transistor array panel of claim 7, wherein the first gate insulation layer does not overlap the source region and the drain region of the semiconductor.

9. The thin film transistor array panel of claim 8, wherein the second diffusion barrier layer covers upper surfaces and lateral surfaces of the source region and the drain region of the semiconductor.

10. The thin film transistor array panel of claim 9, wherein the second diffusion barrier layer is substantially entirely overlapped with the source region and the drain region of the semiconductor area.

11. The thin film transistor array panel of claim 6, wherein the first gate insulation layer is disposed directly on the channel region, the source region, and the drain region of the semiconductor, and

wherein the second diffusion barrier layer is disposed directly on the first gate insulation layer.

12. The thin film transistor array panel of claim 11, wherein the second diffusion barrier layer is substantially entirely overlapped with the source region and the drain region of the semiconductor.

13. The thin film transistor array panel of claim 6, further comprising

a second gate insulation layer disposed on the first gate electrode, the second diffusion barrier layer, and the semiconductor,

wherein the second gate insulation layer is disposed directly on the source region and the drain region of the semiconductor.

14. The thin film transistor array panel of claim 13, wherein the second diffusion barrier layer is partially overlapped with the source region and the drain region of the semiconductor.

15. The thin film transistor array panel of claim 1, further comprising:

a second gate insulation layer disposed on the first gate electrode and the second diffusion barrier layer;

a second gate electrode disposed on the second gate insulation layer; and

an interlayer insulation layer disposed on the second gate electrode and the second gate insulation layer,

wherein the source electrode and the drain electrode are disposed on the interlayer insulation layer.

16. The thin film transistor array panel of claim 15, wherein the second gate insulation layer includes silicon nitride.

17. An organic light emitting diode display comprising:

a substrate;

a semiconductor disposed on the substrate;

a first gate insulation layer disposed on the semiconductor;

a first diffusion barrier layer disposed on the first gate insulation layer;

a second diffusion barrier layer disposed on a lateral surface of the first diffusion barrier layer;

a first gate electrode disposed on the first diffusion barrier layer;

a source electrode and a drain electrode connected to the semiconductor;

a first electrode connected to the drain electrode;

an organic emission layer disposed on the first electrode; and

a second electrode disposed on the organic emission layer,

wherein the first diffusion barrier layer comprises a metal, and the second diffusion barrier layer comprises a metal oxide including the metal.

18. The organic light emitting diode display of claim 17, wherein lateral edges of the first diffusion barrier layer and the first gate electrode are substantially aligned with each other.

19. The organic light emitting diode display of claim 17, wherein

the semiconductor includes an oxide semiconductor material,

the first gate electrode includes copper,

the first diffusion barrier layer includes titanium, and

the second diffusion barrier layer includes titanium oxide.

20. The organic light emitting diode display of claim 17, wherein

the semiconductor includes a channel region, and a source region and a drain region disposed on opposite sides of the channel region,

the first gate insulation layer, the first diffusion barrier layer, and the first gate electrode overlap the channel region of the semiconductor, and

the second diffusion barrier layer overlaps the source region and the drain region of the semiconductor.

* * * * *

专利名称(译)	薄膜晶体管阵列面板和包括其的有机发光二极管显示器		
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摘要(译)

本发明的示例性实施例提供了一种薄膜晶体管阵列面板和包括该薄膜晶体管阵列面板的有机发光二极管显示器，包括基板，设置在基板上的半导体，设置在半导体上的第一栅极绝缘层，以及第一扩散阻挡层设置在第一栅极绝缘层上的层。第二扩散阻挡层设置在第一扩散阻挡层的侧表面上。第一栅电极设置在第一扩散阻挡层上。源电极和漏电极连接到半导体。第一扩散阻挡层包括金属，第二扩散阻挡层包括含金属的金属氧化物。